A Design Framework for Carbon Nanotube Circuits Affixed on DNA Origami Tiles

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SWNT and DNA as elementary nanomaterials

Single-wall carbon nanotubes (SWNTs) can be fabricated either metallic (m) or semiconducting (s). A cross-junction between an m- and s-type SNWTs generates a structure with field effect transistor (FET) behavior [1, 4]. In this way, both p-type and n-type FETs are realizable (a p-type FET is ON when input is "0", while an n-type FET is ON when input is "1"). Moreover, these structures can be affixed on top of DNA origami [2, 5].

Design framework for CNFET circuits

The elements of the circuits are Carbon Nanotube Field Effect Transistors (CNFETs) and Carbon Nanotube Wires (CNW). They are placed on top of different DNA origami tiles which self-assemble into any desired circuit.

Basic elements of the nanocircuits:

- Crossed SWNTs act as p-type and n-type FET;
- Metallic SWNTs act as connecting wires;
- DNA origami structures act as scaffold for circuit assembly

Framework advantages

- The design framework allows a structured and clear design;
- The self-assembly aspects of the manufacturing process are decoupled from the transistor circuit design;
- The design framework supports efficient high-level analysis of the purported circuits, both by computer simulations and by analytical means.

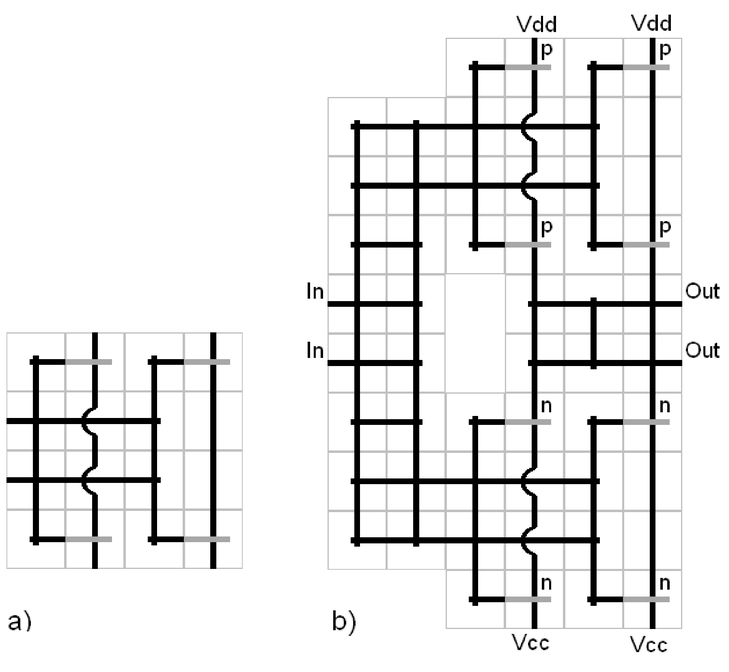
Fault tolerance implementation for CNFET circuits

Due to various assembly faults, an SWNT from a CNFET tile, or from a 4-way CNW junction tile, might be missing. Then, these tiles become straight CNW tiles. Thus, all assembly errors can be treated as tiling errors. In the worst case, a highly altered tile is replaced by the blank tile.

The quadded-transistor structure technique [6] achieves fault tolerance both for transistors and for wires.

- Each CNFET is replaced by four similar ones: two connected in series, and two in parallel.
- Each CNW is replaced by two parallel-paired and bridged CNWs

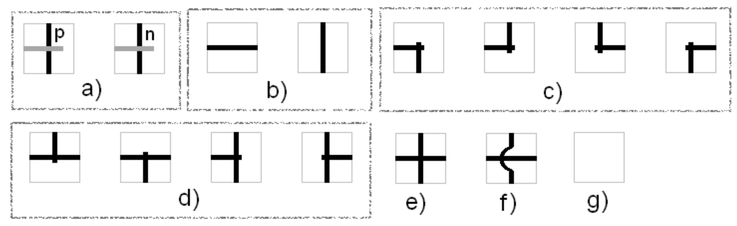
Even if several tiles are erroneous, the circuit will still give the correct output.



a) Implementation of the quadded-transistor structure b) A fault tolerant inverter

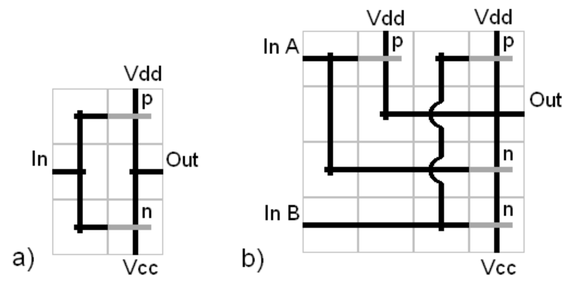
A Universal CNFET Tile Set

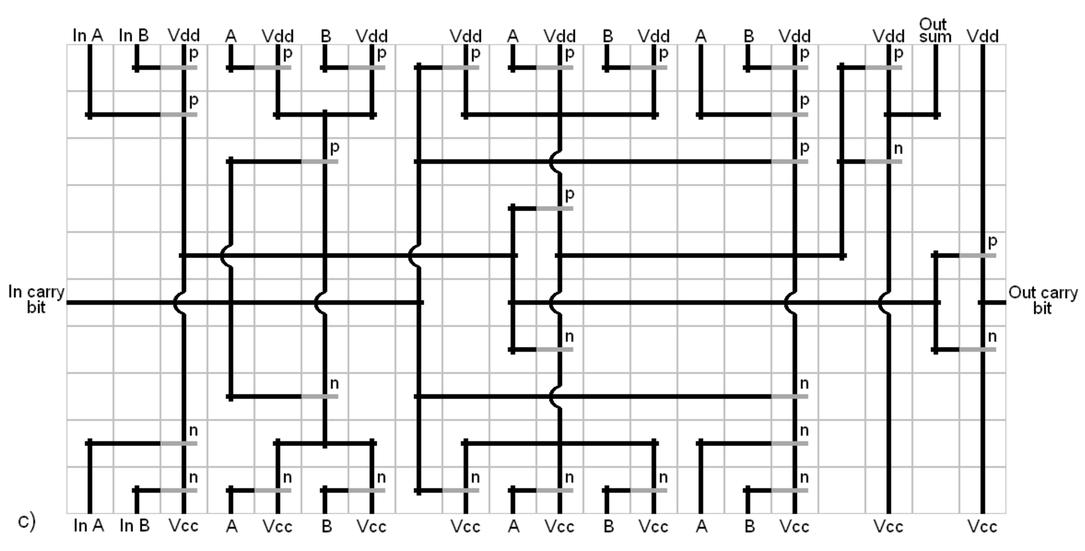
We provide a "universal" set of 14 functionalised DNA origami tiles. With a proper selection of "glues" on the tiles, any desired CNFET circuit can be self-assembled from this basis.



The marks on the tiles indicate the arrangements of the SWNTs affixed on the respective DNA origami: a) p-type and n-type CNFETs, b) straight CNWs, c) corner CNWs, d)-e) 3- and 4-way CNW junctions, f) crossing but non-interacting CNWs, g) blank tile (used for analyzing fault tolerant architectures).

Examples





The design of a) CMOS inverter, b) CMOS NAND gate, and c) CMOS full adder.

Pipeline for CNFET circuit blueprint realization

Given a particular circuit:

- Construct the transistor circuit design using the Universal CNFET Tile Set;
- Compute the optimal number of glues for generating the tile pattern [3];
- Generate appropriate DNA sequences for implementing the glues of the tiles as DNA "sticky ends".

References

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[4] Lee D.S., et al. Fabrication of crossed junctions of semiconducting and metallic carbon nanotubes: a CNT-gated CNT-FET. *J. Nanosci. Nanotechnol.* 6(5) (2006).

[5] Maune T.H., et al. Self-assembly of carbon nanotubes into two-dimensional geometries using DNA origami templates. *J. Nanosci. Nanotechnol.* 6(5) (2006).

[6] J. J. Suran Use of circuit redundancy to increase system reliability. *Int. Solid-State Circuits Conf.* (1964).